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EXAMINER	
CHEN, ERIC BRICE	
ART UNIT	**PAPER NUMBER**
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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/604,056	WILLE ET AL.	
	Examiner	Art Unit	
	Eric B. Chen	1765	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on 3/2/05.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-51 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-51 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102 or 103

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-6, 11, 13-18, 27, 29-32, and 50-51 are rejected under 35 U.S.C. 102(b) as anticipated by or, in the alternative, under 35 U.S.C. 103(a) as obvious over Hussein et al. (U.S. Patent No. 6,365,529).

4. As to claim 1, Hussein discloses a method for forming an etched pattern on a semiconductor substrate, the method comprising the steps of: depositing a thin film (103) on the substrate (100) (column 4, lines 51-53; Figure 1B); depositing a layer of planarizing material (104) on the thin film (103) (column 5, lines 43-51; Figure 1D); depositing a layer of barrier material (108) on the layer of planarizing material (104) (column 10, lines 46-47, lines 55-60); depositing at

least one layer of imaging material (136) on the layer of barrier material (108) (column 6, lines 65-67; Figure 3C); forming at least one first pattern shape (106) in the layers of imaging material (136), barrier material (108) and planarizing material (104) (column 11, lines 19-22; Figures 1E-F); removing the imaging material (136), either after or concurrently with forming the first pattern shape in the planarizing material (column 11, lines 23-24); and transferring the first pattern shape to the thin film (103) (column 11, lines 19-22; Figures 1E-F).

5. Although Hussein discloses that barrier material (108) functions as an anti-reflective layer (column 10, lines 46-47), the reference further discloses that the material comprises either silicon nitride or titanium nitride (column 10, lines 55-60). Thus, Hussein's disclosed anti-reflective layer (108) inherently functions as a diffusion barrier because silicon nitride and titanium nitride are commonly used diffusion barrier materials. *See* Wolf, *Silicon Processing for the VLSI Era*, vol. 1, Lattice Press (1986), page 191; *see also id.*, vol. 4, page 720. In the alternative, applicants' claimed layer, as acting in the capacity of a diffusion barrier, would have obviously have been provided as a result of using Hussein's anti-reflective layer because both layers are composed of the same material and therefore possess the same properties. *See In re Best*, 195 USPQ 430, 433, n.4 (CCPA 1977).

6. As to claim 2, Hussein discloses that at least one second pattern shape (107) is formed in the thin film (103) prior to depositing the layer of planarizing material (104) (column 5, lines 14-15), and the second pattern shape (107) is filled by the planarizing material (104) (column 5, lines 43-45).

7. As to claim 3, Hussein discloses that the thin film (103) is a dielectric material (column 4, lines 51-53).

8. As to claim 4, Hussein discloses that the thin film (103) is a low-k dielectric material (column 4, lines 60-67).

9. As to claim 5, Hussein discloses that the low-k dielectric material has a dielectric constant less than 3.9 (column 4, lines 60-67).

10. As to claim 6, Hussein discloses that the low-k dielectric material has a dielectric constant less than about 3.2 (column 4, lines 60-67).

11. As to claim 11, Hussein discloses that the barrier material (108) comprises a material selected from the group consisting of silicon, silicon nitride, silicon carbide, titanium nitride, and tantalum nitride (column 10, lines 55-60).

12. As to claim 13, Hussein discloses that the step of filling the first pattern shape (106) with a conductive material (column 8, lines 65-66; Figure 1H) after removing the imaging material (136), the barrier material (108) and the planarizing material (104).

13. As to claim 14, Hussein discloses that the conductive material comprises copper (column 8, lines 65-66, column 10, lines 30-31)

14. As to claim 15, Hussein discloses a method for forming a dual damascene interconnect structure on a semiconductor substrate comprising at least one patterned conductor, the method comprising the steps of: depositing a dielectric material (103) on the substrate (100) (column 4, lines 51-53; Figure 1B); forming at least one via (107) in said dielectric material (103) (column 5, lines 14-15), such that at least one of the vias is positioned over the patterned conductor

(Figure 1C); depositing a layer of planarizing material (104) on the dielectric material (103) and in the via (107) (column 5, lines 43-45); depositing a layer of barrier material (108) on the layer of planarizing material (104) (column 10, lines 46-47, lines 55-60; Figure 3B); depositing at least one layer of imaging material (136) on the layer of barrier material (108) (column 6, lines 65-67; Figure 3C); forming at least one trench (106) in the layers of imaging material (136), barrier material (108) and planarizing material (104) (column 11, lines 19-22; Figures 1E-F), such that at least one of the trenches (106) is positioned over the via (107) (Figure 1F); removing the imaging material (136), either after or concurrently with forming the trench (106) in the planarizing material (104) (column 11, lines 23-24); transferring the at least one trench to the dielectric material (103), such that at least one of the trenches (106) is positioned over the via (107) (column 11, lines 19-22; Figure 1F).

15. Although Hussein discloses that barrier material (108) functions as an anti-reflective layer (column 10, lines 46-47), the reference further discloses that the material comprises either silicon nitride or titanium nitride (column 10, lines 55-60). Thus, Hussein's disclosed anti-reflective layer (108) inherently functions as a diffusion barrier because silicon nitride and titanium nitride are commonly used diffusion barrier materials. *See* Wolf, *Silicon Processing for the VLSI Era*, vol. 1, Lattice Press (1986), page 191; *see also id.*, vol. 4, page 720. In the alternative, applicants' claimed layer, as acting in the capacity of a diffusion barrier, would have obviously have been provided as a result of using Hussein's anti-reflective layer because both layers are composed of the same material and

therefore possess the same properties. *See In re Best*, 195 USPQ 430, 433, n.4 (CCPA 1977).

16. As to claim 16, Hussein discloses that the dielectric material (103) is a low-k dielectric material (column 4, lines 60-67).

17. As to claim 17, Hussein discloses that the low-k dielectric material has a dielectric constant less than 3.9 (column 4, lines 60-67).

18. As to claim 18, Hussein discloses that the low-k dielectric material has a dielectric constant less than about 3.2 (column 4, lines 60-67).

19. As to claim 27, Hussein discloses that the barrier material (108) comprises a material selected from the group consisting of silicon, silicon nitride, silicon carbide, titanium nitride, and tantalum nitride (column 10, lines 55-60).

20. As to claim 29, Hussein discloses the step of filling the via (107) and the trench (106) with a conductive material (column 8, lines 65-66; Figure 1H), after removing the imaging material (136), the barrier material (108) and the planarizing material (104).

21. As to claim 30, Hussein discloses that the conductive material comprises copper (column 8, lines 65-66, column 10, lines 30-31).

22. As to claim 31, Hussein discloses that at least one via (107) has a height, and the layer of planarizing material (104) has a thickness of about half the via height to about twice the via height. Hussein discloses that dielectric material (103) has a minimum thickness of 2,000 Å (column 4, lines 66-67) and that via (107) is etched through the entire thickness of the dielectric material (column 5,

lines 14-15). Hussein further discloses that planarizing material (104) has a thickness between 500 and 3,000 Å (column 5, lines 46-48).

23. As to claim 32, Hussein discloses that the layer of barrier material (108) has a thickness of about 50 to 100 nm (column 10, lines 48-49).

24. As to claims 50, Hussein discloses the steps of: removing the barrier layer (108) (column 11, lines 15-19), either after or concurrently with transferring the first pattern shape (106) to the thin film (column 11, lines 19-22); and removing the planarizing material (column 11, lines 31-35).

25. As to claims 51, Hussein discloses the steps of: removing the barrier layer (108) (column 11, lines 15-19), either after or concurrently with transferring the at least one trench (106) to the thin film (column 11, lines 19-22); and removing the planarizing material (column 11, lines 31-35).

26. Claims 12, 28, 33-36, and 45-49 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hussein.

27. As to claims 12, 28, and 46 Hussein does not expressly discloses the steps of: depositing a layer of anti-reflective coating on the barrier material, prior to depositing the layer of imaging material; and removing the anti-reflective coating, either after or concurrently with forming the first pattern shape in the planarizing material. However, Hussein discloses that silicon nitride, silicon carbide, and titanium nitride are suitable inorganic anti-reflective materials (column 10, lines 55-60). Moreover, the purpose of the anti-reflective coating is to reduce the reflection at the wavelength of light used during the subsequent lithography step, thus reducing any adverse effects impacting critical dimension

control (column 10, lines 61-67). Therefore, it would have been obvious to one of ordinary skill in art at the time the invention was made to include the steps of: depositing a layer of anti-reflective coating on the barrier material, prior to depositing the layer of imaging material; and removing the anti-reflective coating, either after or concurrently with forming the first pattern shape in the planarizing material. One who is skilled in the art would be motivated to reduce the reflection at the wavelength of light used during the subsequent lithography step, thus reducing any adverse effects impacting critical dimensions.

28. As to claim 33, Hussein discloses a method for forming a dual damascene interconnect structure on a semiconductor substrate comprising at least one patterned conductor, the method comprising the steps of: depositing a dielectric material (203) on the substrate (200) (Figure 2A); forming at least one trench (206) in the dielectric material (203) (column 9, lines 10-12), such that at least one of the trenches (206) is positioned over the patterned conductor (201) (Figure 2B); depositing a layer of planarizing material (204) on the dielectric material (203) and in the trench (column 9, lines 29-32; Figure 2C); depositing at least one layer of imaging material (250) on the layer of barrier material (column 9, lines 37-38); forming at least one via in the layers of imaging material and planarizing material (column 9, lines 38-40), such that at least one of the via is positioned over the trench and the patterned conductor (Figure 2D); removing the imaging material (250), either after or concurrently with forming the via in the planarizing material (column 9, lines 64-67); transferring the at least one via (207) to the dielectric material (203), such that at least one of the via is

positioned over the trench and the patterned conductor (column 9, lines 38-40; Figure 2E); and removing the planarizing material (column 9, lines 64-67).

29. Hussein does not expressly disclose, for the same embodiment, depositing a layer of barrier material on the layer of planarizing material; and removing the barrier material, either after or concurrently with transferring the at least one via to the dielectric material. However, for a different embodiment, Hussein discloses forming a silicon nitride or titanium nitride (column 10, lines 55-60) inorganic anti-reflective layer (108) over planarizing layer (104) (column 10, lines 46-67). Furthermore, inorganic anti-reflective layer (108) is removed (column 11, lines 15-19) either after or concurrently with transferring the at least one feature to the dielectric material (column 11, lines 19-22). Moreover, the purpose of the anti-reflective coating is to reduce the reflection at the wavelength of light used during the subsequent lithography step, thus reducing any adverse effects impacting critical dimension control (column 10, lines 61-67). Therefore, it would have been obvious to one of ordinary skill in art at the time the invention was made to depositing a layer of anti-reflective coating on the barrier material, prior to depositing the layer of imaging material. One who is skilled in the art would be motivated to reduce the reflection at the wavelength of light used during the subsequent lithography step, thus reducing any adverse effects impacting critical dimensions.

30. Hussein's disclosed anti-reflective layer (108) inherently functions as a diffusion barrier because silicon nitride and titanium nitride are commonly used diffusion barrier materials. *See* Wolf, *Silicon Processing for the VLSI Era*, vol. 1,

Lattice Press (1986), page 191; *see also id.*, vol. 4, page 720. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to deposit a layer of barrier material on the layer of planarizing material; and remove the barrier material, either after or concurrently with transferring the at least one via to the dielectric material.

31. As to claim 34, Hussein discloses that the dielectric material (203) is a low-k dielectric material (column 9, lines 6-10; column 4, lines 60-67).

32. As to claim 35, Hussein discloses that the low-k dielectric material has a dielectric constant less than 3.9 (column 9, lines 6-10; column 4, lines 60-67).

33. As to claim 36, Hussein discloses that the low-k dielectric material has a dielectric constant less than about 3.2 (column 9, lines 6-10; column 4, lines 60-67).

34. As to claim 45, Hussein discloses that the barrier material (108) comprises a material selected from the group consisting of silicon, silicon nitride, silicon carbide, titanium nitride, and tantalum nitride (column 10, lines 55-60).

35. As to claim 47, Hussein discloses the step of filling the via (207) and the trench (206) with a conductive material (column 10, lines 29-31; Figure 2G), after removing the imaging material (250), the barrier material (108) and the planarizing material (204).

36. As to claim 48, Hussein discloses that the conductive material comprises copper (column 10, lines 30-31).

37. As to claim 49, Hussein discloses that the layer of barrier material (108) has a thickness of about 50 to 100 nm (column 10, lines 48-49).

38. Claims 7-8, 20-23, and 38-41 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hussein in view of Lamb III et al. (U.S. Patent No. 6,391,472).

39. As to claims 7, 20, and 38 Hussein does not expressly disclose that the planarizing material is a poly(hydroxystyrene)-based system. Lamb teaches that there is a need in the art for contact and via hole filler materials to provide adequate protection during etching and preventing damage to underlying metal conductors (column 2, lines 14-19). However, if sidewall polymer buildup occurs during etching, this creates an undesirable increase in circuit resistance (column 2, lines 8-12). Moreover, Lamb discloses polymer binders which do not result in undue buildup around the top edge of a via hole or opening (column 2, lines 28-34), including polyhydroxystyrene (column 2, lines 56-61). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use a poly(hydroxystyrene)-based system as a planarizing material. One who is skilled in the art would be motivated to use a resin material that does not result in desirable buildup around the via hole or opening.

40. As to claims 8, 23, and 41, Hussein does not disclose that planarizing material is selected from the group consisting of polyarylsulfones, polyhydroxystyrene-based derivatives, polyimides, polyethers, polyarylenesulfides, polycarbonates, epoxies, epoxyacrylates, polyarylenes, polyarylenevinylenes, polyvinylcarbazole, cyclicolefins, and polyesters. Lamb teaches that there is a need in the art for contact and via hole filler materials to provide adequate protection during etching and preventing damage to underlying

metal conductors (column 2, lines 14-19). However, if sidewall polymer buildup occurs during etching, this creates an undesirable increase in circuit resistance (column 2, lines 8-12). Moreover, Lamb discloses polymer binders which do not result in undue buildup around the top edge of a via hole or opening (column 2, lines 28-34), including polyhydroxystyrene, polycarbonates, epoxies, and polyesters (column 2, lines 56-61). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use a planarizing material selected from the group consisting of polyarylsulfones, polyhydroxystyrene-based derivatives, polyimides, polyethers, polyarylenesulfides, polycarbonates, epoxies, epoxyacrylates, polyarylenes, polyarylenevinylenes, polyvinylcarbazole, cyclicolefins, and polyesters. One who is skilled in the art would be motivated to use a resin material that does not result in desirable buildup around the via hole or opening.

41. As to claims 21 and 39, Hussein does not expressly disclose the step of baking the planarizing material at a temperature of about 200°C to about 250°C, after deposition of the planarizing material. However, Lamb discloses that the poly(hydroxystyrene)-based system has a cross-linking temperature from about 150-220°C (column 3, lines 26-28). Lamb further teaches that to cure the resin, it should be heated at a temperature greater than the cross-linking temperature (column 4, lines 24-28). It should be noted that there is a substantial overlap between Lamb's temperature range and the applicants' range. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the step of baking the planarizing material at a

temperature of about 200°C to about 250°C. One who is skilled in the art would be motivated to cure the resin by heating it to a temperature greater than the cross-linking temperature.

42. As to claims 22 and 40, Hussein does not disclose the step of baking the planarizing material at a temperature of about 225°C, after deposition of the planarizing material. However, Lamb discloses that the poly(hydroxystyrene)-based system has a cross-linking temperature from about 150-220°C (column 3, lines 26-28). Lamb further teaches that to cure the resin, it should be heated at a temperature greater than the cross-linking temperature (column 4, lines 24-28). Applicants' temperature is close enough to Lamb's temperature range, such that similar results would be expected. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the step of baking the planarizing material at a temperature of about 225°C. One who is skilled in the art would be motivated to cure the resin by heating it to a temperature greater than the cross-linking temperature.

43. Claims 9-10, 19, 24-26, 37, and 42-44 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hussein in view of Wolf.

44. As to claims 9, 25, and 43, Hussein does not expressly discloses that barrier material comprises silicon dioxide deposited by plasma-enhanced chemical vapor deposition at a temperature of about 100°C to about 225°C. Wolf teaches that silicon dioxide is suited as a capping layer to prevent outdiffusion, and characterized by uniform thickness and composition, low particulate contamination, good adhesion, low stress, and conformal coverage (vol. 1, page

182). Moreover, Wolf teaches that chemical vapor deposition is a common method of depositing silicon dioxide (vol. 1, pages 182-83) and that a typical deposition temperature for plasma-enhanced chemical vapor deposition is 200°C (vol. 1, Table 2, page 183). It should be noted that the applicants' temperature range overlaps with the typical temperature taught by Wolf. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the diffusion barrier with silicon dioxide deposited by plasma-enhanced chemical vapor deposition at a temperature of about 100°C to about 225°C. One who is skilled in the art would be motivated to select a material commonly used as a diffusion barrier with beneficial characteristics such as uniform thickness and composition, low particulate contamination, good adhesion, low stress, and conformal coverage. Moreover, one who is skilled in the art would be motivated to use an established method for depositing oxide and select deposition temperatures that either overlap or are similar to conventional temperatures.

45. As to claims 10, 26, and 44, Hussein does not expressly discloses that barrier material is deposited by plasma-enhanced chemical vapor deposition at a temperature of about 150°C. Moreover, Wolf teaches that chemical vapor deposition is a common method of depositing silicon dioxide (vol. 1, pages 182-83) and that a typical deposition temperature for plasma-enhanced chemical vapor deposition is 200°C (vol. 1, Table 2, page 183). Although applicants' temperature range is outside the typical temperature taught by Wolf, the temperatures are close enough, such that similar results would be expected.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to deposit the barrier material deposited by plasma-enhanced chemical vapor deposition at a temperature of about 150°C. One who is skilled in the art would be motivated to select an established method for depositing oxide and to select a deposition temperature that is similar to a conventional temperature.

46. As to claims 19 and 37, Hussein does not expressly disclose that the low-k dielectric material is SiCOH deposited by chemical vapor deposition. However, Wolf teaches that SiCOH, deposited by chemical vapor deposition, is a commonly used low-k dielectric material (vol. 4, page 690) for damascene structures (vol. 4, page 689). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use SiCOH as the low-k dielectric material, deposited by chemical vapor deposition. One who is skilled in the art would be motivated to use a commonly used low-k material, which has been successfully implemented for producing damascene structures.

47. As to claims 24 and 42, Hussein does not expressly discloses that the barrier material is silicon dioxide. Wolf teaches that silicon dioxide is suited as a capping layer to prevent outdiffusion, and characterized by uniform thickness and composition, low particulate contamination, good adhesion, low stress, and conformal coverage (vol. 1, page 182). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to select silicon dioxide as a barrier layer material. One who is skilled in the art would be motivated to use a commonly used barrier material with beneficial characteristics

such as uniform thickness and composition, low particulate contamination, good adhesion, low stress, and conformal coverage.

48. Claims 33-36, 42, 45, and 47-49 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Daniels et al. (U.S. Patent No. 6,583,047).

49. As to claim 33, Daniels discloses a method for forming a dual damascene interconnect structure on a semiconductor substrate comprising at least one patterned conductor, the method comprising the steps of: depositing a dielectric material on the substrate (column 15, lines 58-61; Figure 3A); forming at least one trench in the dielectric material (column 15, lines 65-67; column 16, lines 1-2), such that at least one of the trenches is positioned over the patterned conductor (column 14, lines 39-40; lines 47-48); depositing a layer of planarizing material on the dielectric material and in the trench (column 16, lines 3-6; Figure 3D); depositing at least one layer of imaging material on the layer of planarizing material (column 16, lines 6-9; Figure 3E); forming at least one via in the layers of imaging material and planarizing material (column 16, lines 11-13), such that at least one of the vias is positioned over the trench (Figure 3F) and the patterned conductor (column 14, lines 39-40); removing the imaging material, either after or concurrently with forming the via in the planarizing material (column 16, lines 13-16; Figure 3G); transferring the at least one via to the dielectric material (Figure 3F), such that at least one of the vias is positioned over the trench and the patterned conductor (column 14, lines 39-40; lines 47-48); and removing the planarizing material (column 16, lines 13-16; Figure 3F). Daniels does not expressly disclose the steps of: depositing a layer of barrier material on

the layer of planarizing material; depositing at least one layer of imaging material on the layer of barrier material; forming at least one via in the barrier material; and removing the barrier material, either after or concurrently with transferring the at least one via to the dielectric material. However, in a separate embodiment, Daniels teaches that a barrier material may be formed between the photoresist and dielectric (column 17, lines 65-67; column 21, lines 10-12), to prevent adverse reactions between the two layers (column 1, lines 51-62). Therefore, it would have been obvious to one of ordinary skill in the art to deposit a layer of barrier material under the photoresist layer and adapt the process steps to include the barrier material layer. One who is skilled in the art would be motivated to deposit a layer of barrier material under the photoresist layer in order to prevent the occurrence of adverse reactions between layers.

50. As to claim 34, Daniels discloses that the dielectric material is a low-k dielectric material (column 10, lines 56-58).

51. As to claim 35, Daniels discloses that the low-k dielectric material has a dielectric constant less than 3.9 (column 10, lines 58-63).

52. As to claim 36, Daniels discloses that the low-k dielectric material has a dielectric constant less than about 3.2 (column 10, lines 58-63).

53. As to claim 42, Daniels discloses that the barrier material is silicon dioxide (column 17, line 67; column 18, line 1).

54. As to claim 45, Daniels discloses that the barrier material comprises a material selected from the group consisting of silicon, silicon nitride, silicon

carbide, titanium nitride, and tantalum nitride (column 17, lines 65-67; column 18, lines 1-8).

55. As to claim 47, Daniels discloses that step of filling the via and the trench with a conductive material, after removing the imaging material, the barrier material and the planarizing material (column 16, lines 16-19).

56. As to claim 48, Daniels discloses that the conductive material comprises copper (column 10, lines 44-46).

57. As to claim 49, Daniels discloses that the layer of barrier material has a thickness of about 50 to 100 nm (column 21, lines 10-12; lines 28-30).

58. Claims 37 and 43-44 stands rejected under 35 U.S.C. 103(a) as being unpatentable over Daniels in view of in view of Wolf.

59. As to claim 37, Daniels does not expressly disclose that the low-k dielectric material is SiCOH deposited by chemical vapor deposition. However, Wolf teaches that SiCOH, deposited by chemical vapor deposition, is a commonly used low-k dielectric material (vol. 4, page 690) for damascene structures (vol. 4, page 689). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use SiCOH as the low-k dielectric material, deposited by chemical vapor deposition. One who is skilled in the art would be motivated to use a commonly used low-k material, which has been successfully implemented for producing damascene structures.

60. As to claim 43, Daniels does not expressly disclose that the barrier material is deposited by plasma-enhanced chemical vapor deposition at a temperature of about 100°C to about 225°C. Wolf teaches that chemical vapor

deposition is a common method of depositing silicon dioxide (vol. 1, pages 182-83) and that a typical deposition temperature for plasma-enhanced chemical vapor deposition is 200°C (vol. 1, Table 2, page 183). It should be noted that the applicants' temperature range overlaps with the typical temperature taught by Wolf. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Daniels' method with the teachings of Wolf (silicon oxide is deposited by plasma-enhanced chemical vapor deposition at a temperature of about 100°C to about 225°C). One who is skilled in the art would be motivated to select an established method for depositing oxide and to select deposition temperatures that either overlap or are similar to conventional temperatures.

61. As to claim 44, Daniels does not expressly disclose that the barrier material is deposited by plasma-enhanced chemical vapor deposition at a temperature of about 150°C. Wolf teaches that chemical vapor deposition is a common method of depositing silicon dioxide (vol. 1, pages 182-83) and that a typical deposition temperature for plasma-enhanced chemical vapor deposition is 200°C (vol. 1, Table 2, page 183). Although applicants' temperature range is outside the typical temperature taught by Wolf, the temperatures are close enough, such that similar results would be expected. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Daniels' method with the teachings of Wolf (silicon oxide is deposited by plasma-enhanced chemical vapor deposition at a temperature of about 150°C). One who is skilled in the art would be motivated to select an established

method for depositing oxide and to select a deposition temperature that is similar to a conventional temperature.

62. Claims 38-41 are rejected under 35 U.S.C. 103(a) as being unpatentable over Daniels in view of Lamb.

63. As to claim 38, Daniels does not expressly disclose that the planarizing material is a poly(hydroxystyrene)-based system. Lamb teaches that there is a need in the art for contact and via hole filler materials to provide adequate protection during etching and preventing damage to underlying metal conductors (column 2, lines 14-19). However, if sidewall polymer buildup occurs during etching, this creates an undesirable increase in circuit resistance (column 2, lines 8-12). Moreover, Lamb discloses polymer binders which do not result in undue buildup around the top edge of a via hole or opening (column 2, lines 28-34), including polyhydroxystyrene (column 2, lines 56-61). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use a poly(hydroxystyrene)-based system as a planarizing material. One who is skilled in the art would be motivated to use a resin material that does not result in desirable buildup around the via hole or opening.

64. As to claim 39, Daniels does not expressly disclose the step of baking the planarizing material at a temperature of about 200°C to about 250°C, after deposition of the planarizing material. However, Lamb discloses that the poly(hydroxystyrene)-based system has a cross-linking temperature from about 150-220°C (column 3, lines 26-28). Lamb further teaches that to cure the resin, it should be heated at a temperature greater than the cross-linking temperature

(column 4, lines 24-28). It should be noted that there is a substantial overlap between Lamb's temperature range and the applicants' range. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the step of baking the planarizing material at a temperature of about 200°C to about 250°C. One who is skilled in the art would be motivated to cure the resin by heating it to a temperature greater than the cross-linking temperature.

65. As to claim 40, Daniels does not disclose the step of baking the planarizing material at a temperature of about 225°C, after deposition of the planarizing material. However, Lamb discloses that the poly(hydroxystyrene)-based system has a cross-linking temperature from about 150-220°C (column 3, lines 26-28). Lamb further teaches that to cure the resin, it should be heated at a temperature greater than the cross-linking temperature (column 4, lines 24-28). It should be noted that there is a substantial overlap between Lamb's temperature range and the applicants' temperature. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the step of baking the planarizing material at a temperature of about 225°C. One who is skilled in the art would be motivated to cure the resin by heating it to a temperature greater than the cross-linking temperature.

66. As to claim 41, Daniels does not disclose that planarizing material is selected from the group consisting of polyarylsulfones, polyhydroxystyrene-based derivatives, polyimides, polyethers, polyarylenesulfides, polycarbonates, epoxies, epoxyacrylates, polyarylenes, polyarylenevinylenes, polyvinylcarbazole,

cyclicolefins, and polyesters. Lamb teaches that there is a need in the art for contact and via hole filler materials to provide adequate protection during etching and preventing damage to underlying metal conductors (column 2, lines 14-19). However, if sidewall polymer buildup occurs during etching, this creates an undesirable increase in circuit resistance (column 2, lines 8-12). Moreover, Lamb discloses polymer binders which do not result in undue buildup around the top edge of a via hole or opening (column 2, lines 28-34), including polyhydroxystyrene, polycarbonates, epoxies, and polyesters (column 2, lines 56-61). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use a planarizing material selected from the group consisting of polyarylsulfones, polyhydroxystyrene-based derivatives, polyimides, polyethers, polyarylenesulfides, polycarbonates, epoxies, epoxyacrylates, polyarylenes, polyarylenevinylenes, polyvinylcarbazole, cyclicolefins, and polyesters. One who is skilled in the art would be motivated to use a resin material that does not result in desirable buildup around the via hole or opening.

67. Claim 46 is rejected under 35 U.S.C. 103(a) as being unpatentable over Daniels in view of Hussein.

68. As to claim 46, Daniels does not expressly disclose the steps of: depositing a layer of anti-reflective coating on the barrier material, prior to depositing the layer of imaging material; and removing the anti-reflective coating, either after or concurrently with forming the via in the planarizing material. However, Hussein discloses forming an anti-reflective layer (108) directly

underlying imaging material (136) (column 10, lines 46-60; Figure 3C). Moreover, the purpose of the anti-reflective coating is to reduce the reflection at the wavelength of light used during the subsequent lithography step, thus reducing any adverse effects impacting critical dimension control (column 10, lines 61-67). Hussein further teaches removing anti-reflective layer (108) after lithography and etching has been completed (column 11, lines 8-18). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include the steps of: depositing a layer of anti-reflective coating on the barrier material (or directly under the imaging material), prior to depositing the layer of imaging material; and removing the anti-reflective coating, either after or concurrently with forming the via in the planarizing material. One who is skilled in the art would be motivated to reduce the reflection at the wavelength of light used during the subsequent lithography step, thus reducing any adverse effects impacting critical dimensions.

Response to Arguments

69. The rejection of claims 1-6, 11, 13-18, 24, 27, 29-30, and 32 under 35 U.S.C. 102(e) as being anticipated by Lui has been withdrawn in light of Applicants' Declaration under 37 C.F.R. 1.131, filed Mar. 2, 2005. Applicant correctly argues that Lui is not available as prior art against the present application (Applicants' Remarks, page 11). However, upon further consideration, a new ground(s) of rejection is made in view of Hussein.

70. The rejection of claims 7-8, 12, 20-23, and 28 under 35 U.S.C. 103(a) as being unpatentable over Lui in view of Bao has been withdrawn in light of Applicants' Declaration under 37 C.F.R. 1.131, filed Mar. 2, 2005. Applicant correctly argues that Bao is not available as prior art against the present application (Applicants' Remarks, page 12). However, upon further consideration, a new ground(s) of rejection is made in view of Hussein and Lamb.

71. The rejection of claims 9-10, 19, and 25-26 under 35 U.S.C. 103(a) as being unpatentable over Lui in view of Wolf has been withdrawn in light of Applicants' Declaration under 37 C.F.R. 1.131, filed Mar. 2, 2005. Applicant correctly argues that Lui is not available as prior art against the present application (Applicants' Remarks, page 12). However, upon further consideration, a new ground(s) of rejection is made in view of Hussein and Lamb. Because Form PTO-892 identifies two Wolf references, any citations to Wolf in the Office Action mailed Feb. 7, 2005 have been labeled as either as "vol. 1" or "vol. 4" along with the corresponding page number.

72. Applicants' arguments (Applicants' Remarks, page 14), filed Mar. 2, 2005, regarding the rejection of claims 33-36, 42, 45, and 47-49 under 35 U.S.C. 103(a) as being unpatentable over Daniels have been fully considered but they are not persuasive. In response to Applicants' argument that the references fail to show certain features of Applicants' invention, it is noted that the features upon which applicant relies (i.e., complete removal of the barrier material) are not recited in the rejected claims. Although the claims are interpreted in light of the

specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

73. Applicants' arguments (Applicants' Remarks, pages 14-15), filed Mar. 2, 2005, regarding the rejection of claims 37 and 43-44 are rejected under 35 U.S.C. 103(a) as being unpatentable over Daniels in view of Wolf have been fully considered but they are not persuasive, as discussed above.

74. The rejection of claims 38-41 and 46 under 35 U.S.C. 103(a) as being unpatentable over Daniels in view of Wolf, in further view of Bao has been withdrawn in light of Applicants' Declaration under 37 C.F.R. 1.131, filed Mar. 2, 2005. Applicant correctly argues that Bao is not available as prior art against the present application (Applicants' Remarks, page 15). However, upon further consideration, a new ground(s) of rejection is made in view of Hussein and Lamb.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eric B. Chen whose telephone number is (571) 272-2947. The examiner can normally be reached on Monday through Friday, 8AM to 4:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nadine G. Norton can be reached on (571) 272-1465. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

EBC EBC
April 18, 2005

NADINE G. NORTON
SUPERVISORY PATENT EXAMINER